IN THE CLAIMS

Upon entry of the present amendment, the status of the claims will be as is shown below. This listing of claims replaces all previous versions and listings of claims in the present application.

Claims 1-12 (Cancelled)

13. (New) A memory circuit for temporarily storing information symbols to receive a signal according to a CDMA system which allows multi-code communication and to perform coherent detection using a pilot symbol, the memory circuit comprising:

a plurality of electrically independent memory blocks, each memory block being associated with a code in the multi-code communication and a slot in a reception signal; and

a memory interface that periodically performs data write and data read with said plurality of blocks so as not to allow write access and read access to one memory block at a same time;

wherein the memory interface selectively accesses a memory block associated with a slot subject to coherent detection and a memory block associated with a slot currently being received.

14. (New) The memory circuit of claim 13, further comprising:

a memory operation controller that sets memory blocks to which no access is made in a low power consumption mode.

15. (New) The memory circuit according to claim 14, wherein the low power consumption mode of the memory blocks is implemented by stopping supply of an

operating clock.

16. (New) An information symbol storage memory access control method, comprising:

providing an information symbol storage memory in which a memory area is divided into a plurality of electrically independent memory blocks based on at least one of information about the number of multi-codes and slot information;

selectively accessing a memory block associated with a slot subject to coherent detection and a memory block associated with a slot currently being received; and

periodically performing data write and data read with the plurality of blocks so as not to allow write access and read access to one memory block at a same time.

17. (New) The memory circuit of claim 13, wherein said memory interface periodically performs data write and data read with said plurality of blocks so as not to allow write access to one memory block during a read access to said one memory block, and so as not to allow a read access to said one memory block during a write access to said one memory block".

18. (New) The information symbol storage memory access control method of claim 16, wherein said periodically performing comprises periodically performing data write and data read with said plurality of blocks so as not to allow write access to one memory block during a read access to said one memory block, and so as not to allow a read access to said one memory block during a write access to said one memory block